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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,581	12/12/2003	Satoru Konishi	H-1125	8605

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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,581	KONISHI ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,6-12,14-18 and 23-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-4,6-12 and 23-34* is/are allowed.

6)☒ Claim(s) *14,18,35,37 and 38* is/are rejected.

7)☒ Claim(s) *15-17 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: Photocopy of Electronic Materials and Processes Handbook, 2nd ed., 1994 (4 sheets including pp.1.10-1.11)..

DETAILED ACTION

1. The present Office Action is responsive to Applicant's amended Response filed March 15, 2006. The Examiner acknowledges the amendments to Claims 2, 6, 14, 23 and 35, and the cancellation of Claims 1, 5, 13 and 19-22. Claims 2-4, 6-12, 14-18 and 23-38 remain pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Hofstee et al. (US 2002/0074668 A1) Chan et al. (US 6,849,940 B1)

Electronic Materials and Processes Handbook, 2nd ed., McGraw-Hill, Inc., 1994, Harper & Sampson, editors, pp.1.10 and 1.11 (hereinafter referenced as "*EMPH*").

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 14, 35, 37 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Hofstee et al.

As to Claim 14, Hofstee et al. discloses: a module board having wiring 214 over an upper surface thereof and external electrode terminals (to which BGA elements 216 are connected) over a lower surface thereof (Fig. 2; last three lines of paragraph [0021]); a first semiconductor chip 206-1 and a second semiconductor chip 206-2 over which active elements are formed (Fig. 2); and a first integrated passive device 204 (i.e., decoupling capacitor; Fig. 5; paragraphs [0024] and [0025]), wherein the first semiconductor chip 206-1 and the second semiconductor chip 206-2 are arranged at an upper surface side of the module board with a predetermined distance therebetween (Fig. 2); and wherein the first integrated passive device 204 is arranged over an upper surface of the first semiconductor chip 206-1 (Figs. 2 and 5).

As to Claim 35, Hofstee et al. discloses: a module board having wiring 214 over an upper surface thereof and external electrode terminals (to which BGA elements 216 are connected) over a lower surface thereof (Fig. 2; last three lines of paragraph [0021]); a first semiconductor chip 206-1 and a second semiconductor chip 206-2 formed the module board and including active elements (Fig. 2); and an integrated passive device 204 (i.e., decoupling capacitor; Fig. 5; paragraphs [0024] and [0025]), wherein one semiconductor chip 206-1 out of the first and second semiconductor chips 206-1 and 206-2 and the integrated passive device 204 are mounted over an upper surface of the module board in an overlapped manner (Fig. 2), and wherein the semiconductor module includes a heat radiation pad 228 formed over a lower surface of the module board and a plurality of vias 226 which are formed such that the vias vertically penetrate the module board and have lower ends thereof connected to the

heat radiation pad 228, and the second semiconductor chip 206-2 is arranged over the plurality of vias 226 (Fig. 2; paragraph [0020]).

As to Claim 37, Hofstee et al. further discloses, in Fig. 2, that first semiconductor chip 206-1, second semiconductor chip 206-2 and integrated passive device 204 are covered with a sealing portion 202 made of insulating resin (i.e., plastic; paragraph [0016]). *Examiner's Note*: *EMPH* (see section 2, above) discloses, on p.1.10, a definition of plastic as "[a]n organic resin or polymer;" and on p.1.11, discloses a definition of *resin* as "[a] high-molecular weight organic material with no sharp melting point. For current purposes, the terms *resin*, *polymer*, and *plastic* can be used interchangeably." Consequently, the present claim has been rejected with multiple (two) references, wherein *EMPH* explains the meaning of the term "plastic" disclosed in Hofstee et al., in accordance with the multiple rejection practice outlined in MPEP § 2131.01, part II.

As to Claim 38, Hofstee et al. further discloses, in Fig. 2, that end portions of the sealing portion 202 are not positioned outside the end portions of the module board.

5. Claims 14 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al.

As to Claim 14, Chan et al. discloses, in Fig. 5: a module board 503 having wiring 516 over an upper surface thereof and external electrode terminals (not shown, but corresponding to and receiving solder balls 527) over a lower surface thereof; a first semiconductor chip 507 and a second semiconductor chip 508 over which active elements are formed (col.6: 38-41); and a first integrated passive device 510 (col.6: 32-

34), wherein the first semiconductor chip 507 and the second semiconductor chip 508 are arranged at an upper surface side of the module board 503 with a predetermined distance therebetween (Fig. 5), and the first integrated passive device 510 is arranged over an upper surface of the first semiconductor chip 507 (Fig. 5).

As to Claim 18, Chan et al. further discloses a second integrated passive device 511 (col.6: 32-34) is mounted over (i.e., "above") an upper surface of the module board 503, and the second integrated passive device 511 is mounted over (i.e., "on") an upper surface of the second semiconductor chip 508 (Fig. 5). *Examiner's Note*: The term "over" does not require physical or electrical contact; rather,"over" encompasses both concepts of "on" and "above," as indicated.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 35, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al.

A) As to Claim 35:

I. Chan et al. discloses, in Fig. 5: a module board 503 having wiring 516 over an upper surface thereof and external electrode terminals (not shown, but corresponding to and receiving solder balls 527) over a lower surface thereof; a first semiconductor chip 507 and a second semiconductor chip 508 formed over the module board 503 and including active elements (col.6: 38-41); and an integrated passive device 510 (col.6: 32-34), wherein one semiconductor chip 507 out of the firs semiconductor chip 507 and second semiconductor chip 508 and the integrated passive device 510 are mounted over an upper surface of module board 503 in an overlapped manner (Fig. 5).

II. Chan et al. discloses a heat spreader 501 (Fig. 5; col.6: 29-30) but does not teach a heat radiation pad formed over a lower surface of module board 503 and vias vertically penetrating module board 503 and having lower ends thereof connected to the heat radiation pad, such that the second semiconductor chip 508 is arranged over the plurality of vias, the vias thus functioning as thermal vias drawing heat away from chip 508 toward the heat radiation pad for dissipation from the package.

III. Hofstee et al., like Chan et al., discloses first and second semiconductor chips 206-1 and 206-2, an integrated passive device 204 mounted on chips 206-1 and 206-2, and a heat spreader 218, and further discloses a heat radiation pad 228 formed over a

lower surface of the module board which, in conjunction with the vias vertically penetrating the module board and having lower ends thereof connected to the heat radiation pad 228, serves to draw heat away from semiconductor chips 206-1 and 206-2 in order to dissipate heat away from the chips 206-1, 206-2 and the package 200 to prevent chip overheating and thereby ensuring package performance reliability (paragraphs [0020] and [0021]).

IV. Since both Chan et al. and Hofstee et al. are both in the same electronics packaging art of multichip modules, then the additional heat sinking structures of a heat radiation pad on at least the lower surface of the module board and vertical vias penetrating the module board and having lower ends thereof connected to the heat radiation pad to function as heat sinking thermal vias, as taught by Hofstee et al., would have been readily recognized for the same purpose in the pertinent art of Chan et al.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module board of Chan et al. to include a heat radiation pad formed over a lower surface of module board 503 and vias vertically penetrating module board 503 and having lower ends thereof connected to the heat radiation pad, such that the second semiconductor chip 508 is arranged over the plurality of vias, the vias thus functioning as thermal vias drawing heat away from chip 508 toward the heat radiation pad for dissipation from the chips and the package in order to ensure package performance reliability, as taught by Hofstee et al.

B) As to Claim 37, modified Chan et al. further discloses first semiconductor chip 507, second semiconductor chip 508 and integrated passive device 510 are covered with a sealing portion made of insulating resin 505 (Fig. 5; col.6: 27-32).

C) As to Claim 38, modified Chan et al. further discloses that end portions of the sealing portion 505 are not positioned outside the end portions of module board 503 (Fig. 5).

Allowable Subject Matter

9. Claims 2-4, 6-12, 23-24, 25-29, 30-32 and 33-34 have been allowed.

10. Claims 15-17 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner's Remarks

11. The indicated allowability of Claims 14 and 35 is withdrawn in view of the newly discovered reference(s) to Hofstee et al. (US 2002/0074668 A1) and Chan et al. (US 6,849,940 B1). Rejections based on the newly cited references are set forth, above, in the present Office Action. Accordingly, the present Office Action has been made NON-FINAL.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Warner (US 6,856,007 B2) discloses an embodiment in Fig. 23 comprising a module board 1018 with wiring 1022 over an upper surface but no wiring or external electrode terminals on a lower surface; rather, the mounting of module board 1018 onto a system circuit board (such as circuit board 1112 in Fig. 24) is done through the solder mass in the hole of the module board 1018 (such as the solder 150 in the hole 124 of module board 142 in the similar embodiment of Fig. 3; col.10: 37-53). Fig. 21 discloses a different embodiment with semiconductor surface acoustic wave chips 914 and 954, and adjacent integrated passive devices 915 and 956, wherein the module board 918 has wiring 938 on an upper surface and external electrode terminals 922 on a lower surface thereof (col.19: 41-50; note that in line 49, element "906" should have been labeled as --954--). However, the structure of the embodiment of Fig. 23 includes wiring 1026 to the *top* surface of the module board 1018 and, like its variant embodiment in Fig. 24 (wherein no external terminals on a bottom surface of the module board 1118 are apparently necessary due to the solder connections 1179) makes connections to an external circuit board through the above-mentioned solder masses, unlike the embodiment of Fig. 21, wherein the semiconductor SAW chips are connected by wiring 926 to the *bottom* surface of module board 918, and terminals 922 on the bottom surface are connected to the wiring 926 to establish external connection to another circuit board or device. There is no motivation to add external terminals (such as

terminals 922 on the bottom surface of module board 918 in the embodiment of Fig. 21) to the bottom surface of module board 1018 in the embodiment of Fig. 23, which is structurally distinct from the embodiment of Fig. 21, as is required by Applicant's Claim 14. However, Warner does teach, in Fig. 23, at least two semiconductor chips 1014 (amplifiers; col.14: 32-44; at least two such chips: col.21: 26-29) mounted on the module board 1018 and an integrated passive device 1015 (col.20: 64-67) mounted on at least one of the chips 1014 in an overlapped manner (col.20: 55-col.21: 3).

b) Ho et al. (US 2005/0122698 A1), in Figs. 15 and 16, does not teach that one of the semiconductor chips 12 and an integrated passive device 25 are mounted over an upper surface of the module in an overlapped manner; Figs. 15 and 16 show chips 12 and integrated passive devices (IPD) 24 wherein a chip 12 and IPD 24 are not overlapped with each other and therefore does not meet the requirements of Applicant's Claim 2. Figs. 15 and 16 show chips 12 formed over the module board 46/42 and the first (larger) chip 12 is mounted over the second (smaller) chip 12 but Ho et al. does not teach that the second (smaller) chip 12 has a heat value (i.e., amount of heat dissipated in operation) greater than the heat value of first (larger) chip 12 and therefore does not meet the requirements of Applicant's Claim 6. Figs. 15 and 16 do not teach the first IPD 24 is arranged over an upper surface of a first semiconductor chip 12, as required by Applicant's Claim 14. Ho et al. does not teach an inter-stage matching circuit provided between semiconductor chips 12 comprised of the IPD 24, as required by Applicant's Claims 23, 25, 30 and 33. Ho et al. does not teach that one of the semiconductor chips 12 and an integrated passive device 25 are mounted over an upper surface of the

module in an overlapped manner and does not teach that the vias that vertically penetrate the module board 46/42 have lower ends connected to heat radiation pad 31, as required by Applicant's Claim 35.

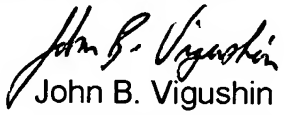
c) Ference et al. (US 6,265,771 B1) discloses a first semiconductor chip 16, a second semiconductor chip 12, a module board 42d, the first chip 16 and second chip 12 mounted in an overlapped manner and thermal vias 46 vertically penetrating the module board to draw heat away from the second chip 12 to the solder bumps 48, and through the solder bumps 48 to the next level of packaging. The thermal vias 46 in conjunction with solder bumps 48 perform the thermal transfer function for chip 12 (Figs. 5a,b). Ference et al., alone, does not teach or fairly suggest modifying the disclosed thermal transfer arrangement by replacing solder bumps 48 on the lower surface of module board 42d with a heat radiating pad, as required by Applicant's Claim 35.

d) Suzuki et al. (US 6,930,334 B2) discloses, in Figs. 4 and 5, a module board 40, a semiconductor chip 50, two integrated passive devices 60 and 70 (with integrated passive elements 61 and 71, respectively), a ground plate 41 on a lower surface of module board 40, ground vias 42 having one end thereof connected to the ground plate 41 (col.7: 6-11). No explicit teaching of thermal transfer by way of ground vias 42 and ground plate 41 but such heat transfer would be inherent in the grounded vias 42 and plate 41, wherein the ground plate would function as a heat radiation pad. Note that Ference et al. (US 6,265,711 B1) discloses that a ground plane functions as a heat transfer element (col.3: 48-53).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
June 09, 2006